CLAIMS

What is claimed is:

1. A Clock Data Model (CDM) for use with a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution, the method comprising:

partitioning the complete clock net into a global clock net and a plurality of local clock nets;

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

combining the plurality of simulations to form the complete clock net; and

storing the plurality of simulations in the Clock Data Model.

2. The CDM as defined in claim 1, wherein partitioning comprises breaking the complete clock net into equal sized parts according to rectangular grid coordinates.

3. The CDM as defined in claim 1, wherein the method further comprises breaking at least one of the plurality of local clock nets down into at least one sub-local clock net.

4. The CDM as defined in claim 3, wherein the method further comprises simulating the at least one sub-local clock net prior to simulating the corresponding local clock net.

5. The CDM as defined in claim 1, wherein at least two of the plurality of local clock nets are simulated in parallel.

6. The CDM as defined in claim 1, wherein simulating each of the plurality of local clock nets comprises:

extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database;

extracting component values of the elements of the local clock net from the microprocessor network database;

simulating the local clock net based on the layout and the component values; and

extracting a load of the local clock net on the global clock net.

7. The CDM as defined in claim 6, wherein simulating the local clock net comprises assuming that the clock arrival times from the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net.

8. The CDM as defined in claim 1, wherein simulating the global clock net comprises:

extracting the layout of the global clock net from a microprocessor network database;

extracting component values of the elements of the global clock net from the microprocessor network database;

inserting the simulated loads of the plurality of local clock nets; and

simulating the global clock net based on the layout, the component values, and the simulated local clock net loads.

9. The CDM as defined in claim 1, wherein the method further comprises evaluating the complete clock net to determine whether the results converge.

10. The CDM as defined in claim 9, wherein, if the results do not converge, the method further comprises:

assuming that clock arrival times are those calculated for the simulated global clock net;

re-simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net;

re-simulating the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets; and

combining the simulations and re-simulations to form the complete clock net.

11. The CDM as defined in claim 10, wherein re-simulating at least one of the plurality of local clock nets comprises:

re-simulating the at least one local clock net based on the layout, the component values, and the calculated clock arrival times; and

extracting a load of the at least one local clock net on the global clock net.

12. The CDM as defined in claim 11, wherein the method further comprises re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net.

13. The CDM as defined in claim 10, wherein re-simulating the global clock net comprises:

inserting the simulated or re-simulated loads of the plurality of local clock nets; and

re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads.

14. The CDM as defined in claim 10, wherein the method further comprises storing the plurality of re-simulations in the Clock Data Model.

15. A Clock Data Model (CDM) for use with a system for determining clock insertion delays for a microprocessor design having grid-based clock distribution, the system comprising means for partitioning the complete clock net into a global clock net and a plurality of local clock nets, means for simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net, means for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets, and means for combining the plurality of simulations to form the complete clock net, the CDM comprising:

means for storing the plurality of simulation results.

16. The CDM as defined in claim 15, further comprising means for collecting all of the information created during the plurality of simulations.

17. The CDM as defined in claim 15, further comprising means for retrieving all of the information created during the plurality of simulations.

18. The CDM as defined in claim 15, further comprising means for querying all of the information created during the plurality of simulations.

19. The CDM as defined in claim 15, further comprising a timing tool interface to provide accurate clock arrival times for each clocked element in the microprocessor design.

20. The CDM as defined in claim 15, wherein the system further comprises means for evaluating the complete clock net to determine whether the results converge, means for assuming that clock arrival times are those calculated for the simulated global clock net, means for re-simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, means for re-simulating the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets, and means for combining the simulations and re-simulations to form the complete clock net and wherein the CDM further comprises means for storing the plurality of re-simulation results.

21. A Clock Data Model (CDM) for use with a system for determining clock insertion delays for a microprocessor design having grid-based clock distribution, the system comprising a

partitioner for horizontally and vertically partitioning the complete clock net into a global clock net and a plurality of local clock nets, at least one local clock net simulator for simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, a global clock net simulator for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets, and a merging unit for combining the plurality of simulations to form the complete clock net, the CDM comprising:

a memory for storing the plurality of simulation results.

22. The CDM as defined in claim 21, further comprising means for collecting all of the information created during the plurality of simulations.

23. The CDM as defined in claim 21, further comprising means for retrieving all of the information created during the plurality of simulations.

24. The CDM as defined in claim 21, further comprising means for querying all of the information created during the plurality of simulations.

25. The CDM as defined in claim 21, further comprising a timing tool interface to provide accurate clock arrival times for each clocked element in the microprocessor design.

26. The CDM as defined in claim 21, wherein the system further comprises a convergence evaluator for evaluating the complete clock net to determine whether the results converge and, when the results are found not to converge, the apparatus assumes that clock

arrival times are those calculated for the simulated global clock net, the at least one local clock net simulator re-simulates at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, the global clock net simulator re-simulates the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets, and the merging unit combines the simulations and re-simulations to form the complete clock net and wherein the CDM further comprises a memory for storing the plurality of re-simulation results.